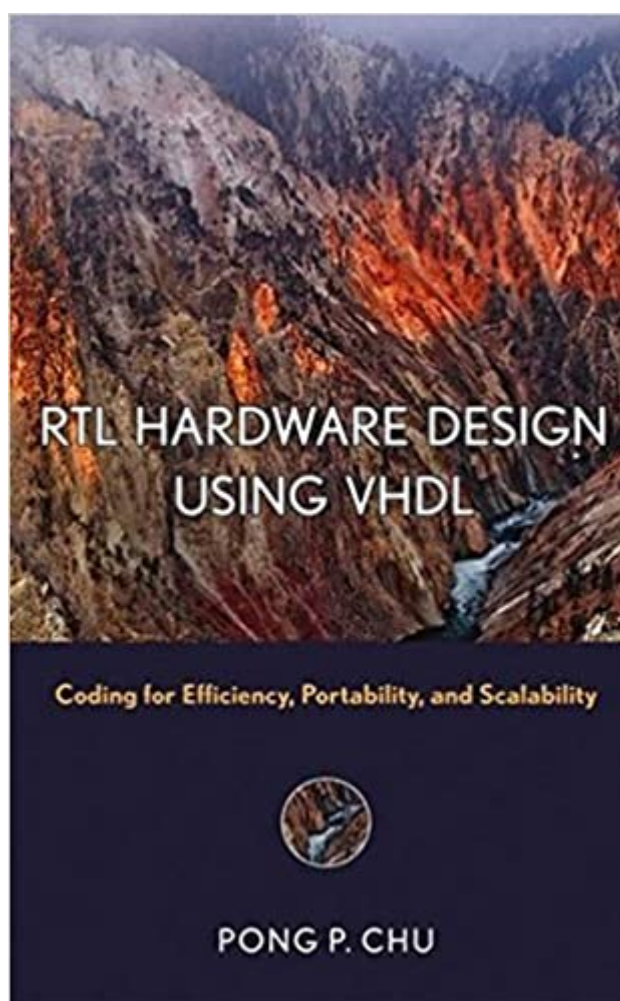The book was found

RTL Hardware Design Using VHDL: Coding For Efficiency, Portability, And Scalability

Synopsis

The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient, portable, and scalable Register Transfer Level (RTL) digital circuits using the VHDL hardware description language and synthesis software. Focusing on the module-level design, which is composed of functional units, routing circuit, and storage, the book illustrates the relationship between the VHDL constructs and the underlying hardware components, and shows how to develop codes that faithfully reflect the module-level design and can be synthesized into efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDL constructs and hardware components * Conceptual diagrams that illustrate the realization of VHDL codes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce design concepts, procedures, and techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs and coding * One chapter covering the synchronization and interface between multiple clock domains Although the focus of the book is RTL synthesis, it also examines the synthesis task from the perspective of the overall development process. Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation, verification, and testing needs, and can be easily incorporated into a larger system or reused. Discussion is independent of technology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practical examples, this is an excellent textbook for upper-level undergraduate or graduate courses in advanced digital logic. Engineers who need to make effective use of today's synthesis software and FPGA devices should also refer to this book.

Book Information

Hardcover: 694 pages

Publisher: Wiley-IEEE Press; 1 edition (April 10, 2006)

Language: English

ISBN-10: 0471720925

ISBN-13: 978-0471720928

Product Dimensions: 7.3 x 1.6 x 10.3 inches

Shipping Weight: 2.9 pounds (View shipping rates and policies)

Average Customer Review: 4.9 out of 5 stars   12 customer reviews

Best Sellers Rank: #593,794 in Books (See Top 100 in Books)   #33 inÃ Â Books > Engineering & Transportation > Engineering > Electrical & Electronics > Circuits > Logic   #184 inÃ Â Books >

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The skills and guidance needed to master RTL hardware design   This book teaches readers how to systematically design efficient, portable, and scalable Register Transfer Level (RTL) digital circuits using the VHDL hardware description language and synthesis software. Focusing on the module-level design, which is composed of functional units, routing circuit, and storage, the book illustrates the relationship between the VHDL constructs and the underlying hardware components, and shows how to develop codes that faithfully reflect the module-level design and can be synthesized into efficient gate-level implementation. Several unique features distinguish the book: Coding style that shows a clear relationship between VHDL constructs and hardware components Conceptual diagrams that illustrate the realization of VHDL codes Emphasis on the code reuse Practical examples that demonstrate and reinforce design concepts, procedures, and techniques Two chapters on realizing sequential algorithms in hardware Two chapters on scalable and parameterized designs and coding One chapter covering the synchronization and interface between multiple clock domains Although the focus of the book is RTL synthesis, it also examines the synthesis task from the perspective of the overall development process. Readers learn good design practices and guidelines to ensure that an RTL design can accommodate future simulation, verification, and testing needs, and can be easily incorporated into a larger system or reused. Discussion is independent of technology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practical examples, this is an excellent textbook for upper-level undergraduate or graduate courses in advanced digital logic. Engineers who need to make effective use of today's synthesis software and FPGA devices should also refer to this book.

PONG P. CHU, PhD, is Associate Professor in the Department of Electrical and Computer Engineering, Cleveland State University. He has received grants from both NASA and the National Science Foundation, and has taught undergraduate and graduate-level digital systems and computer architecture courses for more than a decade.

The world is well populated with books on elementary logic design,Ã Â Katz's being one of the good ones. Such books present all the basics of hardware logic, registers, computer arithmetic, and maybe a little about a popular hardware description language (HDL), Verilog or VHDL. Then there

are the language books that take basic logic concepts and show how to render them in one of the HDLs. Unfortunately, there's not much out there for the student who's mastered the basics, but isn't ready to dive in at the deep end of computer architecture.Chu's book meets the needs of that advancing student better than any other I know. After introductory chapters that orient the reader and set expectations, Chu dives in with a quick tour of VHDL basics. These 'basics', by the way, cover more detail than some entire texts. The next chapters cover principles and practice of combinational and sequential circuits, state machine design, register transfer level (RTL) design, and hierarchical design, with emphasis throughout on timing and efficient design. For example, sharing of functional units comes up as a topic in itself, something that arises in practice but rarely in the classroom. Toward the end, Chu presents the best discussion of parameterized design I've seen, including fairly advanced use of 'generate' statements and VHDL's alternative architectures. The last chapter covers design considerations for clock distribution and for crossing between clock domains, topics that arise in every non-trivial design and that continue to cause problems for designers.This book covers its topics better than any other I know. The beginning logic designer's first course has been well covered, and (except for use of HDLs) hasn't changed all that much since about 1980. The digital world has changed dramatically, though, and this book does a great job starting where other texts leave off.- wiredweird

Needed this book for an upper level undergraduate class on digital design. I am very glad that I had it, since the teacher was not the best at teaching and there was a little bit of a communication barrier. This book does a good job of teaching VHDL in regards to the RTL level. Which if you are unfamiliar is basically combining adders, memories, clocks, and registers together to create things from processor cores to VGA controllers. The book will be best utilized with some form of FPGA trainer board that you can implement the examples on and reinforce your knowledge by creating small projects.

This is a textbook for a university course I'm taking now. I have some background in integration and verification with Verilog from work, but little RTL design. I'd taken a VHDL course way back in my undergrad days and really not liked it at the time, partly due to the terrible textbook way back then. This book is great for learning the VHDL language in a practical usage way. The author doesn't seem to dwell on all possibilities of the language, his focus seems to be on current recommended methods of doing things, and has lots of examples. We have an FPGA based project due most every week, and I'm finding that most of the problems I struggle with at first are discussed in this

book, and get me going. I really enjoy the presentation, and I feel that I will be a much better Verilog designer as well. I just wish that, like some of his other books, there was a Verilog equivalent of this book.

I enjoyed the book and gained a fairly robust knowledge of VHDL from it, though I do wish they would consolidate more tables of information, perhaps in an appendix in the back.However, I just thought I would note that this book is really poorly bound. I have yet to hear of one where the binding wasn't falling apart, amongst my classmates and others. I know this isn't a game-changing factor, but thought it was worth mentioning.

Pong P. Chu use a very clear language and goes right in the subject.The book explains in details how to develop and understand a good VHDL code, it shows the hardware that's going to be synthesized by your VHDL code, showing the best practices and the advantages/disadvantages of VHDL constructs and the trade offs (speed/area/propagation delay etc.)

Book was in very very good condition. 100% satisfied. I feel like product was exceeded my expectations.I would recommend this seller.

Good item & fast delivery!

An excellent resource.

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